High performance, low power consumption

PowerPC 750 Microprocessors

Highlights

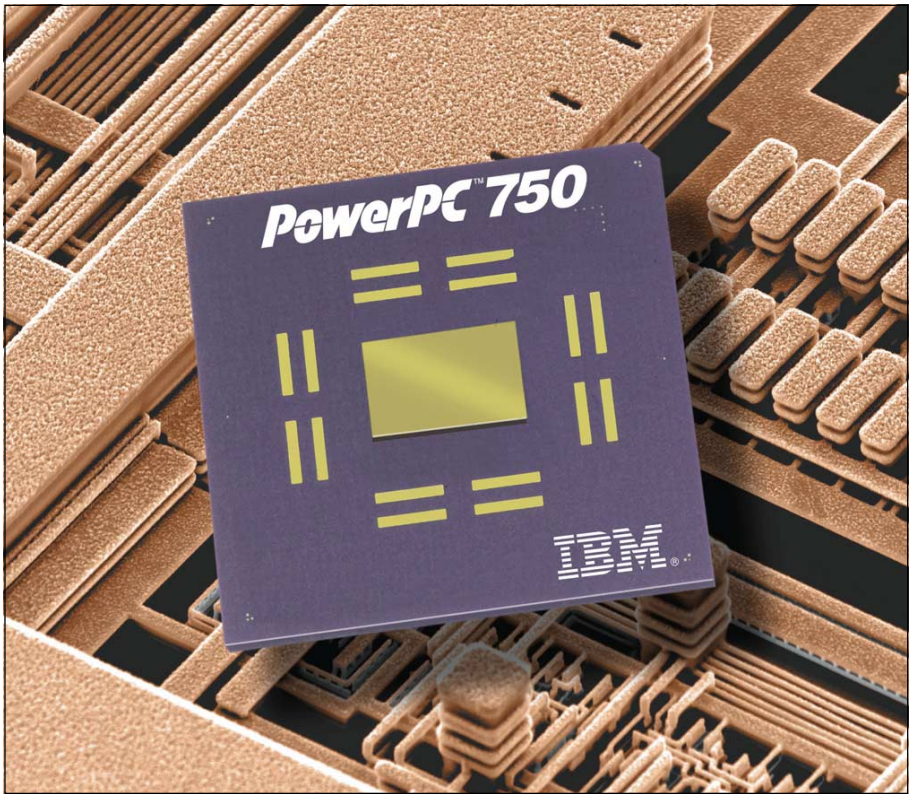
IBM® Microelectronics' family of high-performance PowerPC 750™ microprocessors now includes new copper-based 300 MHz-500 MHz processors that deliver significantly higher clock speeds and lower power consumption. The first microprocessors featuring IBM's advanced CMOS 7S copper technology, these state-of-the-art devices are designed for compliance with the PowerPC™ Architecture.

The new microprocessors extend the IBM PowerPC 750 microprocessor family to provide solutions for an even wider range of applications—from high-performance desktop systems to cost-sensitive embedded devices. PowerPC 750 microprocessors offer a performance advantage across a range of applications, including products such as VME boards and upgrade cards. The PowerPC architecture and performance-enhancing features, including an L2 cache controller, contribute to this competitive advantage.

Versatility and high performance

The IBM PowerPC 750 microprocessor is a high-performance, versatile engine for a wide range of applications, ranging from mainstream desktop systems to high-end workstations and mobile devices. A 32-bit implementation of the PowerPC Reduced Instruction Set (RISC) architecture, the PowerPC 750 microprocessor combines state-of-the-art CMOS 7S process technology and advanced design features to deliver high clock rates, low power and a small die size.

The PowerPC 750 microprocessor's integrated L2 cache controller, when combined with high-speed L2 cache, increases overall system performance across a range of applications. At 500 MHz, the PowerPC 750 microprocessor delivers an estimated performance of 23.9 SPECint95 and 14.6 SPECfp95 when configured with 1 MB of L2 cache. The PowerPC 750 processor uses 6 Watts or less power which enables more efficient, compact designs for mobile and other low-power applications.



The IBM PowerPC 750 Microprocessor features advanced CMOS 7S copper technology.

Because all PowerPC 750 microprocessors share the same powerful architecture, footprint and I/O voltage, manufacturers can take advantage of faster microprocessors in their products without redesigning their boards. They can increase the speed and breadth of their product offerings while maintaining compatibility with current and previous-generation PowerPC 750 microprocessor designs.

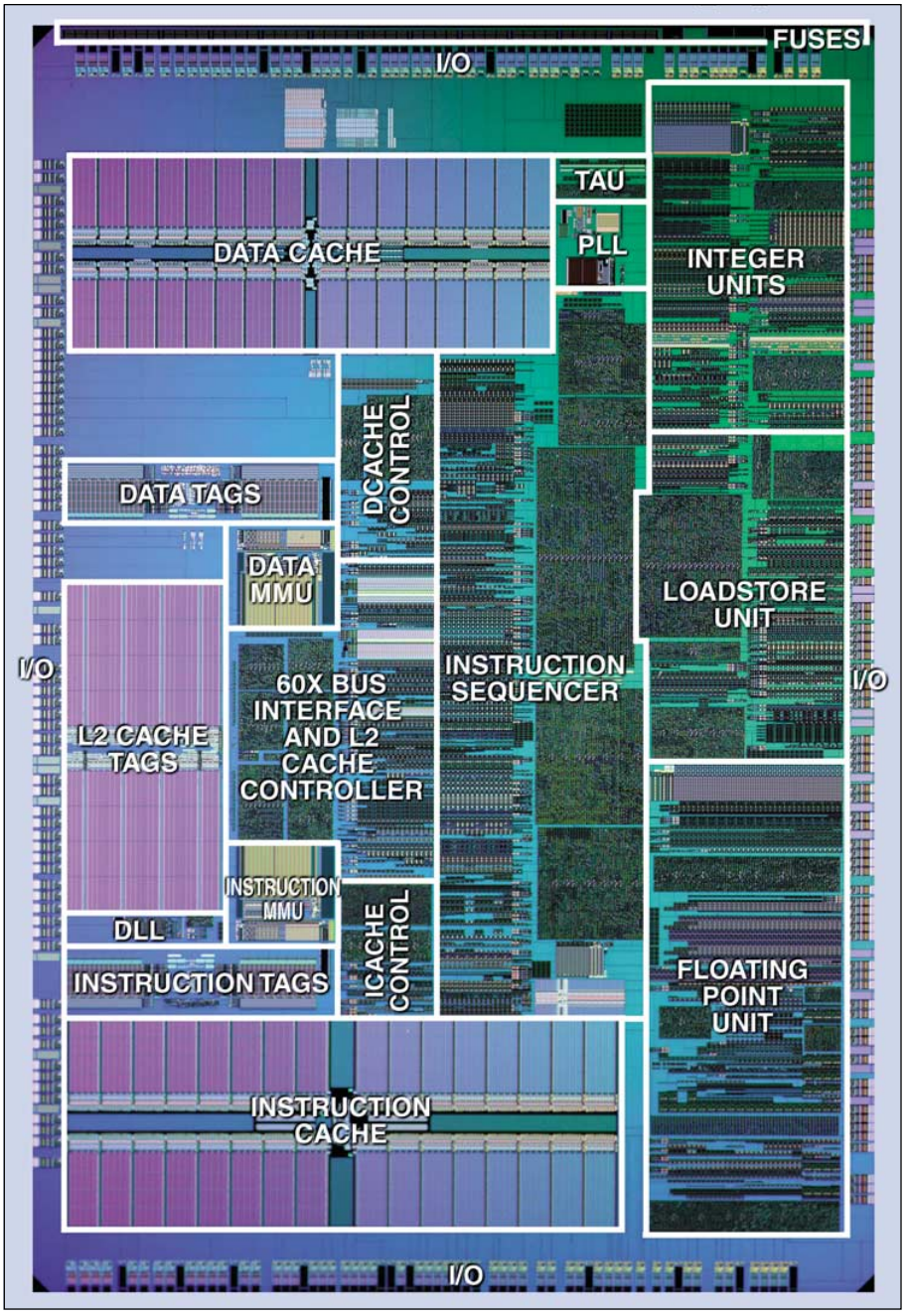
The combination of these leadership attributes makes the PowerPC 750 microprocessor the premier solution for diverse applications.

IBM's State-of-the-Art Copper-Based Process

Using copper instead of aluminum to create circuitry on silicon wafers is a major milestone in semiconductor technology. With the PowerPC 750 300-500 MHz microprocessors, IBM Microelectronics is the first to implement this technology in production processors.

IBM's new copper-based CMOS 7S process technology represents extensive research and development over many years. While copper has long been recognized as a superior electrical conductor, it has been difficult to adapt to semiconductor manufacturing, leaving aluminum as the material of choice for more than thirty years.

IBM's CMOS 7S process overcomes this challenge. This copper-based process enhances the electrical properties of circuits and provides advances in miniaturization that allow computer intelligence to be built into products that are smaller, faster, integrate more complex functions, and require less cooling.



PowerPC 750 Chip Overlay

Functional Description:

Power Management Unit
- Static low-power design
- Dynamic power management
- Integrated thermal management assist unit

Level 2 (L2) Cache Interface
- Internal L2 cache controller and 4-K-entry tags
- Supports 256-KB, 512-KB, and 1-MB 2-way set associative L2 cache
- Copy-back or write-through data cache
- 64-byte (256 KB/512 KB) and 128-byte (1 MB) sectored line size
- Support up to 233 MHz SRAMs
- Parity on interface

Instruction Fetching & Branch Unit
- 4 instructions fetched per clock
- 64-entry BTIC
- 512-entry BHT

Dispatch Unit
- Dispatches 2 instructions per cycle
- 4-stage pipeline: fetch, dispatch, execute, and complete

Load/Store Unit
- One cycle cache access
- Executes cache and TLB instructions
- Alignment and number denormalization
- Hit under reload instruction

Fixed-Point Execution Unit
- One cycle add, subtract, shift, or rotate
- Hardware multiply and divide
- Thirty-two, 32-bit general purpose registers

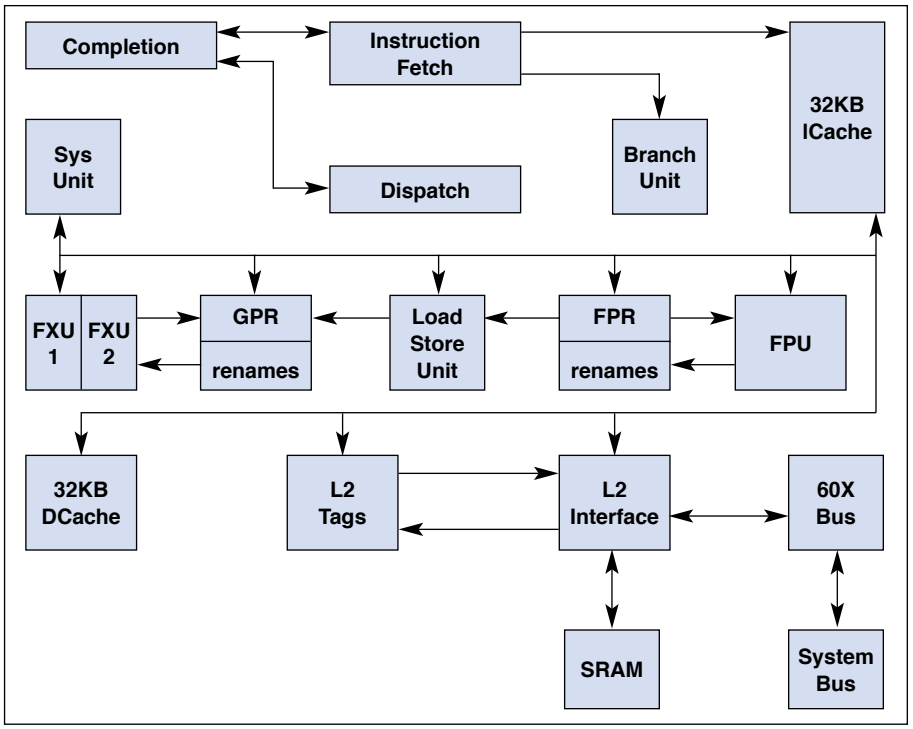
Floating-Point Execution Unit (FPU)
- Optimized for single-precision multiply/add
- IEEE-754 standard single-and double-precision floating point arithmetic
- Thirty-two, 64-bit floating point registers

System Unit
- Executes condition register logical, special register transfer, and other system instructions
- Executes integer add/compare instructions

Memory Management Unit
- 52-bit virtual and 32-bit real addressing
- 8 block address translation registers
- 128-entry, 2-way data and instruction TLB
- Fast-trap mechanism for software reload TLB
- Support for big/little-endian addressing

Cache Unit
- 32-KB, 32-byte line, 8-way set associative instruction cache
- 32-KB, 32-byte line, 8-way set associative data cache
- 3-state coherency (MEI)
- Physically tagged and addressed
- Copy-back or write-through data cache
- Hardware support for data coherency

Bus Interface Unit
- General purpose interface for a wide range of system configurations
- 32-bit address and 64-bit data bus
- Powerful diagnostic and test interface through the Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface
- Parity checking on bus
- Fast reset due to Level Sensitive Scan Design (LSSD)



PowerPC 750 Overview

Specifications	PID 8t				PID 8p					
CPU speed	233-300 MHz				300-500 MHz					
Technology (min.)	0.26 µm / 0.18 L_{eff} - CMOS technology 5 levels of metal				0.20 µm / 0.12 L_{eff} - CMOS copper technology 6 levels of metal					
Die size	7.56 mm x 8.79 mm (67 mm^2)				5.14 mm x 7.78 mm (40 mm^2)					
Number of transistors	6.35 million				6.35 million					
Performance (est)[1]										
Internal (MHz)	300	266	250	233	500	466	450	400	350	333
System bus (MHz)	100	66	83	66	100	83+	100	100	100	83
L2 bus (MHz)	150	133	125	117	250	233	225	200	175	166
SPECint95_Peak	14.8	12.8	12.3	11.0	23.9	21.8	21.4	19.2	16.6	16.0
SPECint95_Base	13.8	12.0	11.5	10.5	22.3	20.5	20.0	18.0	15.7	15.0
SPECfp95_Peak	11.4	8.7	9.5	8.0	14.6	12.6	13.8	13.1	12.0	10.9
SPECfp95_Base	11.0	8.5	9.2	7.7	14.1	12.3	13.3	12.7	11.6	10.6
CPU bus ratio	3X, 3.5X, 4X, 4.5X, 5X, 5.5X, 6X, 6.5X, 7X, 7.5X, 8X				3X, 3.5X, 4X, 4.5X, 5X, 5.5X, 6X, 6.5X, 7X, 7.5X, 8X, 10X[3]					
L1 cache size	32 KB Instruction, 32 KB Data				32 KB Instruction, 32 KB Data					
L2 cache size	Supports 256 KB, 512 KB or 1 MB				Supports 256 KB, 512 KB or 1 MB					
Signal I/Os	267				267					
Power supply[2]	2.5 V to 2.75 V core, 3.3 V +/-5% I/O				2.0 V to 2.1 V core, 3.3 V +/-5% I/O 2.0 V to 2.1 V core, 2.5 V +/-5% I/O[3] 2.0 V to 2.1 V core, 1.8 V +/-5% I/O[3]					
Power dissipation Typ. (est)[2]	5.6 W @ 233 MHz 6.5 W @ 266 MHz 6.7 W @ 275 MHz 7.3 W @ 300 MHz				4.1 W @ 333 MHz 4.7 W @ 400 MHz 5.2 W @ 450 MHz 5.5 W @ 466 MHz 6.0 W @ 500 MHz					
Temperature range[2]	0°-105° C				0°-105° C					
Packaging	Ball Grid Array (360 pins)				Ball Grid Array (360 pins)					

[1] *Estimates with 1 MB L2 cache*
[2] *See datasheet specification for more detailed information.*
[3] *Available on revision 3.x or higher*

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